Strategies for Accelerating Advanced Design, Verification & Test
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Tom Beckley, Senior VP – Custom IC, IC Packaging, PCB & Analysis
Frank Schirrmmeister – Senior Group Director, Solutions
Trends in Electronics and System Design

2020
- Edge-to-Cloud and 5G
- Specialized SoCs
- Artificial Intelligence

2020
- Parallel and Distributed
- Full-Flow Solutions
- Deep Learning

1960
- Moore’s Law
The Morphing of Moore’s Law

• Moore’s Law driving the semi market for decades
• CMOS scaling limit approaching at ~1-2nm
• Companies will add value with advanced packaging
• International Technology Roadmap for Semiconductors changes charter to Heterogenous Integration Roadmap

Gordon Moore – Moore’s Law (1965)
SoC & Systems challenge: H/W, S/W co-development & co-verification

Development Costs

- Software
- Verification
- Physical
- Architecture
- IP qualification

Rapidly Accelerating Chip Costs

Source: IBS July 2019
Nonetheless, Semiconductor Investment Is Accelerating

- Domain-Specific Computing
- System Company Verticalization
  - Custom Silicon, 3DIC, PCBs
- New Silicon Startups, China
- Electronification of New Industries
  - Auto, Aerospace, Industrial, Medical

Strong Design Activity

Source: IBS
Cadence: Intelligent System Design Strategy

**Intelligence Performance**
- Intelligent platforms in end products
- Breakthrough user experiences
- Compute optimized for application workloads

**System Performance**
- Compliance of electromagnetic, thermal, etc.
- Throughput of secure software
- High-performance RF design

**Silicon Performance**
- Analog and digital computation acceleration
- Silicon reliability in advanced-process nodes
- Billion-gate design and verification throughput
From IC to System: Re-architecting the Virtuoso Design Platform

New Virtuoso Design Platform
Innovations for the next wave of analog and system design

Advanced Node Support Down to 3nm
Advanced Design Methodologies Including ML/AI Automation, RF, and Photonics
Enhanced System Design Platform Enabling 2.5D/3D Heterogenous Systems
Everything Wireless: High-Frequency 5G RF Design

Accelerate innovation in comms, A&D, auto and industrial
Multi-Physics System Analysis
SI, PI, EM and Thermal Signoff

IC Design
- Digital IC
- Custom IP
- 2.5D/3D ICs

System Design
- Automotive
- Communications
- Aerospace

Multi-Physics System Simulations
- Voltus™
- Celsius™
- EMX™
- Clarity™
- Sigrity™

Innovus Virtuoso OrbitIO

Signoff

Allegro AWR OrCAD
Successful design: synthesis of information, experience and soon ML/AI, however…

- Information is spread in multiple systems
- Design data is complex to manage
- Reuse is required but time consuming
- Huge volumes of valuable data are produced and discarded along the way
- Tools for cross-domain collaboration are lacking

“Workers, on average, spend 36 percent of their day looking for and consolidating information. But 44 percent of the time, they can’t find the information.”

Source: cmswire.com
Cadence and National Instruments Partnership
Design to Test Flow

Behavioral System Models
Design & Verification
Pre-Silicon Chip Validation
Silicon Bring-up Characterization
Production Test

Behavioral System Models
Spec Capture
Spec Compliance
Coverage Analysis
Status Dashboard

Specification Compliance Management

Data Management Services
Data Lake Storage

Data Management
Data Visualization, Analysis and Reporting

Digital
always@ck
B <= A;
C <= B;
D <= C;

Analog

Specification Compliance Management
AI/ML for Electronics Design?

Checkers

\[10^{31}\]

# of states

Go

\[10^{360}\]

# of states

IC Design

\[10^{8000+}\]

# of states
Automation of IC, Package and Board Design

Analog IC Design
- Front-End Design
  - Schematic
  - Circuit Optimization
  - Floorplanning
  - Placement
  - Routing
  - Finishing and Signoff

PCB / Package Design
- Front-End Design
  - Schematic
  - Trace Optimization
  - Boardplanning
  - Placement
  - Routing
  - Finishing and Signoff

Automate production of IC, package, and PCB while meeting design goals.
Cadence Intelligent System Design Strategy

Cloud Enabled — Partnerships with Ecosystem Leaders

AI, ML and computation software

Investing in Systems / More than Moore

Executing on core EDA / Moore’s Law